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Description

METHOD FOR AVOIDING OXIDE UNDERCUT DURING PRE-SILICIDE CLEAN FOR THIN SPACER FETs

BACKGROUND OF INVENTION

[0001] The present invention relates to complementary metal oxide semiconductor (CMOS) devices, and more particularly to a process and structure for forming a metal oxide semiconductor field effect transistor (MOSFET) implementing thin sidewall spacer geometries.

[0002] Figures 1(a)-1(e) depict cross-section views of a portion of a semiconductor device manufactured in accordance with conventional processing techniques. As shown in Figure 1(a), a semiconductor device 10 is formed on a wafer. The device includes a substrate 12 and a patterned gate stack 15 formed thereon. Each patterned gate stack 15 may be formed of a gate material such as polycrystalline silicon, for example, and as conventionally known, the gate 15 is formed on a thin gate dielectric layer 20

previously formed on top of the substrate 12. Prior to the formation of low resistivity cobalt, titanium, or nickel silicide contacts with active device regions 16, 18 and gate 15 of the semiconductor device 10, thin nitride spacers are first formed on each gate sidewall. Typically, as shown in Figure 1(a), a dielectric etch stop layer 25, ranging from about 10Å-300Åin thickness, but preferably 50Å-150Å, is first deposited on the thin gate oxide layer 20 over the substrate surfaces and the patterned gate stack 15. While this dielectric etch stop prevents recessing of the substrate during reactive ion etching (RIE) of the spacer, it has the disadvantage of being susceptible to removal or undercut during the extensive preclean that must be utilized prior to silicide formation.

[0003] Then, as shown in Figure 1(b), an additional dielectric layer 30 is deposited on the patterned gate stack and active device regions. This additional dielectric layer is typically formed of a nitride material.

[0004] While this dielectric etch stop prevents recessing of the substrate during spacer RIE, it has the disadvantage of being susceptible to removal or undercut during the extensive pre-clean that must be utilized prior to silicide formation.

[0005] As shown in Figure 1(c), a RIE process is performed, resulting in the formation of vertical nitride spacers 35a, 35b on each gate wall. Prior to metal deposition, which may be titanium, cobalt or nickel, a lengthy oxide strip process is performed to prepare the surface for the silicide formation. This oxide strip is crucial to achieving a defect free silicide. However, as illustrated in Figure 1(d), the problem with this lengthy oxide strip is that the dielectric etch stop beneath the spacers 25 becomes severely undercut at regions 40a, 40b. The resultant oxide loss or undercut gives rise to the following problems: 1) the barrier nitride layer 50 that is ultimately deposited, as shown in Figure 1(e), will be in contact with the gate dielectric edge 17, thus degrading gate dielectric reliability; 2) the silicide in the source/drain regions 60a,b (not shown) may come into contact with the gate dielectric at the gate conductor edge, which would create a diffusion to gate short); and, 3) the degree of undercut will vary significantly from lot to lot. These aforementioned problems are particularly acute for transistors with the thin spacer geometries required for(which becoming continued CMOS scaling.

[0006] Thin sidewall spacer geometries are becoming increas-

ingly important aspects of high performance MOSFET design. Thin spacers allow the silicide to come into close proximity to the extension edge near the channel, thereby decreasing MOSFET series resistance and enhancing drive current. The implementation of a spacer etch process (specifically RIE) benefits substantially from an underlying dielectric layer (typically oxide) beneath the nitride spacer film. This dielectric serves as an etch stop for the nitride spacer RIE. Without this etch stop in place, the spacer RIE would create a recess in the underlying substrate, degrading the MOSFET series resistance, and in the case of thin SOI substrates, reducing the amount of silicon available for the silicide process.

[0007] In order to avoid the problems associated with thin spacer geometries on thin SOI, it would be extremely desirable to provide a method for avoiding the oxide undercut when performing the oxide removal step during the pre-silicide clean.

SUMMARY OF INVENTION

[0008] It is thus an object of the present invention to provide a method for avoiding the dielectric, e.g., oxide, undercut when performing the clean step prior to silicide formation, particularly for thin spacer MOSFETs.

[0009] In accordance with this objective, it has been found that the formation of a thin nitride plug encapsulating and sealing a segment of the dielectric etch stop layer underlying the vertical spacer elements will avoid the aforementioned undercut and associated problems.

[0010] A preferred aspect of the present invention thus relates to a method for forming a CMOS device comprising the steps of: (a) providing a patterned gate stack region on the surface of a semiconductor substrate, the patterned gate stack including gate dielectric and exposed vertical sidewalls; (b) forming a dielectric etch stop layer over the gate region, exposed vertical sidewalls, and substrate surfaces; (c) forming a spacer element at each vertical sidewall, the spacer comprising of a nitride layer; (d) removing the dielectric (oxide) etch stop layer using an etch process such that a portion of the dielectric layer underlying each spacer remains; (e) forming a thin nitride layer over the gate region, the spacer elements at each vertical sidewall, and substrate surfaces; (f) etching said nitride plug layer such that a nitride plug layer remains to encapsulate and seal at least a portion of the dielectric that exists beneath the spacer; (g) performing a pre-silicide clean process for removing any material remaining from the substrate and

gate conductor surfaces that may hinder silicide formation, wherein dielectric undercut is prevented by the provision of said nitride plug layer that forms an etch barrier to protect the dielectric layer beneath the spacer elements.

[0011] There are two variations to step (d) above which will be further defined here.

[0012] In the first variation of the invention, the dielectric layer removal (step (d)) includes implementing a dry etch process. For example, a RIE process may be used for the dry oxide etch. This RIE process would be selective and anisotropic such that the vertical edge of the said dielectric layer underlying the spacer that is perpendicular to the wafer surface is aligned with the vertical edge of the vertical nitride spacer element furthest from the gate. Another example of a dry process that may be used for the oxide removal is chemical downstream etching (CDE). reactive ion etching ()CDE is not necessarily anisotropic, so the edge of the dielectric layer after CDE may or may not be vertical, and may be aligned with the vertical edge of the vertical nitride spacer element furthest from the gate or may be slightly recessed closer to the gate.

[0013] In a second variation of the invention, the dielectric layer

removal (step (d)) includes implementing a wet etch process, selective such that the dielectric layer underlying the spacer is pulled back toward the gate and out of alignment with the far edge of the vertical nitride spacer element.

[0014] In either variation, the nitride plug effectively seals the portion of the dielectric (oxide) layer underlying the spacer elements to prevent the oxide removal and undercut caused by the pre-silicide cleaning process.

[0015] Also, for either variation (wet or dry removal of the oxide), the subsequent processing is similar.

[0016] There are two variations to step (f) above which are now defined. In the first variation, the nitride etch described in step (f) above is performed with a dry etch, such as RIE or CDE. Nitride is selectively removed from the source/drain regions and the top of the gate, but at least a portion of the nitride plug layer remains beside the edge of the dielectric layer. This nitride etch variation is compatible with both the oxide etch variations described above.

[0017] In the second variation, the nitride etch described in step (f) is performed with a wet or liquid phase etch. The wet nitride etch removes nitride from the source/drain regions and atop the gate, while retaining at least a portion of the

nitride plug adjacent to the dielectric etch stop to block lateral oxide etching during the silicide preclean. This nitride etch variation is compatible both with CDE in the first variation of step (d) above and the wet oxide etch described in the second variation of step (d) above.

Brief Description of Drawings

[0018] Further features, aspects and advantages of the apparatus and methods of the present invention will become better understood with regard to the following description, appended claims, and the accompanying drawings where:

[0019] Figures 1(a)-1(e) are cross-sectional views showing the CMOS processing steps according to a prior art method.

[0020] Figures 2(a)-2(h) are cross-sectional views showing the basic processing steps according to a first embodiment of the present invention; and,

[0021] Figures 3(a)-3(h) are cross-sectional views showing the basic processing steps according to a second embodiment of the present invention.

Detailed Description

[0022] Fgures 2(a)-2(h) depict the methodology for avoiding oxide undercut when performing a pre-silicide clean step to remove residual material from the silicon surfaces (either

source/drain or gate regions). This methodology enables the formation of transistors with thin spacer geometries for improving FET series resistance.

[0023] The various processing steps and materials used in fabricating the CMOS device of the present invention, together with various embodiments thereof, will now be described in greater detail by the discussion that follows.

[0024] Figure 2(a) illustrates an initial structure that is employed in the present invention. Specifically, the initial structure shown in Figure 2(a) comprises a semiconductor substrate 12 having a patterned gate stack 15 formed on portions of the semiconductor substrate. In accordance with the present invention, each patterned gate stack includes a gate dielectric 20, gate conductor 15 formed atop the gate dielectric, and an additional dielectric etch stop material atop the gate conductor and substrate regions.

[0025] The structure shown in Figure 2(a) is comprised of conventional materials well known in the art, and it is fabricated utilizing processing steps that are also well known in the art. For example, semiconductor substrate 12 may comprise any semiconducting material including, but not limited to: Si, Ge, SiGe, GaAs, InAs, InP, and all other III/V semiconductor compounds. Semiconductor substrate 12

may also include a layered substrate comprising the same or different semiconducting material, e.g., Si/Si or Si/SiGe, silicon-on-insulator (SOI), strained silicon, or strained silicon on insulator. The substrate may be of n- or p-type (or a combination thereof) depending on the desired devices to be fabricated.

[0026] Additionally, semiconductor substrate 12 may contain active device regions, wiring regions, isolation regions or other like regions that are typically present in CMOS devices. For clarity, these regions are not shown in the drawings, but are nevertheless meant to be included within region 12. In two highly preferred embodiments of the present invention, semiconductor substrate 12 is comprised of Si or SOI. With an SOI substrate, the CMOS device of the present invention is fabricated on the thin Si layer that is present above a buried oxide (BOX) region.

[0027] A layer of gate dielectric material 20, such as an oxide, nitride, oxynitride, high-K material, or any combination and multilayer thereof, is then formed on a surface of semiconductor substrate 12 utilizing conventional processes well known in the art. For example, the gate dielectric layer may be formed by a thermal growing process such as oxidation, nitridation, plasma-assisted nitrida-

tion, or oxynitridation, or alternatively by utilizing a deposition process such as chemical vapor deposition (CVD), plasma-assisted CVD, evaporation or chemical solution deposition.

[0028] After forming gate dielectric 20 on the semiconductor substrate 12, a gate conductor 15 is formed on top of the gate dielectric. The term "gate conductor"a s used herein denotes a conductive material, a material that can be made conductive via a subsequent process such as ion implantation or silicidation, or any combination thereof. The gate is then patterned utilizing conventional lithography and etching processes well known in the art. Next, a dielectric etch stop layer 25 is formed on top of the patterned gate conductor. The dielectric etch stop or capping layer 25 is deposited atop the substrate 12 and gate stack 15. In a preferred embodiment, the capping layer 25 is an oxide, ranging from about 10Å-300Å in thickness, and formed utilizing a conventional deposition process such as, though not limited to, CVD, plasma-assisted CVD (PECVD), or ozone-assisted CVD. Alternatively, a conventional thermal growing process such as oxidation may be used in forming the dielectric capping layer 25.

[0029] Next, and as illustrated in Figures 2(b) and 2(c), spacer el-

ements 35a, 35b are formed on the gate sidewalls. Spacer formation begins with the deposition of a nitride film 30 over the dielectric etch stop layer on the patterned gate stack, the gate sidewalls, and the substrate surfaces. The nitride thickness is 700Å or less, and in the case of this invention is further preferred to be 500 Åor less. It is understood that these thickness values are exemplary and that other thickness regimes are also contemplated in the present invention. The composition of the nitride layer can represent any suitable stoichiometry or combination of nitrogen and silicon. The deposition process can include any of the numerous methods known in the art, such as, though not restricted to, PECVD, rapid thermal CVD (RTCVD), or low pressure CVD (LPCVD). After depositing the nitride layer 30 (via chemical vapor deposition or a similar conformal deposition process) on the structure shown in Figure 2(a), the vertical gate wall spacers 35a, 35b are then formed using a highly directional, anisotropic spacer etch, such as RIE. The nitride layer is etched, selective to the underlying dielectric etch stop layer 25, to leave the vertical nitride spacers layer 35a, 35b.

[0030] The key elements of the process are now shown in Figure

2(d) 2(f) whereby after spacer formation, the dielectric etch stop layer 25 remaining on the substrate 12 is first removed by an oxide etch process. This etch can be either dry (RIE or CDE) or wet, as conventionally known. In Figure 2(d), there is depicted the RIE example for removing the remaining dielectric etch stop layer 25 save for a small portion of cap dielectric underlying the vertical nitride spacers. Once the dielectric RIE is complete, as shown in Figure 2(d), the edges of the dielectric etch stop edges 38a, 38b under the vertical spacers, i.e., edges 38a, 38b, will be flush with the vertical edge of the spacer. Next, as shown in Figure 2(e), a thin nitride "plug" layer 40 is deposited over the remaining structure including the exposed gate and substrate surfaces. Preferably the thin nitride plug is 100Åor less in thickness and may include, though not limited to, Si_3N_4, Si_xN_y, carbon-containing Si_xN_y, an oxynitride, or a carbon-containing oxynitride. After deposition, the nitride "plug" layer 40 is etched using an anisotropic dry etch which removes the plug layer from the substrate surfaces and the top of the gate, as shown in Figure 2(f). As a result of this process, thin vertical nitride portions 45a, 45b remain that function to seal the respective underlying dielectric etch stop edges 38a, 38b.

If CDE is used instead of RIE to etch the dielectric etch stop layer, the edge of the etch stop may be slightly recessed with respect to the vertical spacer edge. In this case, a wet etch may be used to remove the nitride "plug" layer from the substrate surfaces and the top of the gate, leaving behind a nitride "plug"t o block the dielectric etch stop from subsequent lateral etching. Once the dielectric edges are sealed, a lengthy oxide strip may be performed as depicted in Figure 2(g) as part of the subsequent silicide preclean without the creation of an oxide undercut in the etch stop layer.

[0031] That is, prior to the metal deposition for silicide formation, a series of wet cleans, dry cleans, or other physical cleaning techniques, may be implemented to remove contaminants such as: resist residuals, any remaining oxides formed during plasma cleans/strips, implant residuals, metals, and particles from the surface of the silicon wafer.

[0032] All three of the above-mentioned problems highlighted in the prior art process depicted in Figures 1(a)-1(d) for the conventional CMOS process are solved.

[0033] As shown in Figure 2(h), with spacers and nitride plug layers in place, it is understood that source/drain regions (not shown) may be formed by conventional techniques,

e.g., ion implantation into the surface of semiconductor substrate 12 utilizing a conventional ion implantation process well known in the art. It is understood, however, that at any point during the process source/drain regions may be formed. Further, it is noted that at this point of the present invention, it is also possible to implant dopants within the gate material. Various ion implantation conditions may be used in forming the deep source/drain regions within the substrate. In one embodiment, the source/drain regions may be activated at this point of the present invention utilizing conventional activation annealing conditions well known to those skilled in the art. However, it is highly preferred to delay the activation of the source/drain regions until after shallow junction regions have been formed in the substrate.

[0034] Finally, silicide contacts 60a, 60b may be formed on portions of the semiconductor substrate 12 for contact with the respective source/drain regions. Specifically, the silicide contacts may be formed utilizing a conventional silicidation process which includes the steps of depositing a layer of refractory metal, such as Ti, Ni, Co, or metal alloy on the exposed surfaces of the semiconductor substrate, annealing the layer of refractory metal under conditions

that are capable of converting said refractory metal layer into a refractory metal silicide layer, and, if needed, removing any un-reacted refractory metal from the structure that was not converted into a silicide layer. Typical annealing temperatures used in forming the silicide contacts are known to skilled artisans. Note that because of the nitride spacers and nitride plug, the silicide contacts may be self-aligned to any deep junction vertical edge present in the underlying substrate.

[0035] Note that in the preferred embodiment of the present invention, as depicted in Figure 2(h), a silicide region 70 is also formed atop the patterned gate stack region.

[0036] Finally, a contact etch stop (or barrier) layer 80 is deposited as a precursor to further CMOS processing, as shown in Figure 2(h).

[0037] As mentioned hereinabove with respect to Figure 2(d), the oxide cap layer 25 remaining on the substrate 12 is removed by an oxide etch process which may be either dry (RIE or CDE) as shown in Figure 2(d) or wet, as now described with respect to Figures 3(d)-3(h). With respect to the second variation of the present invention, steps depicted in Figures 3(a)-3(c) are the same as explained herein with respect to Figures 2(a)-2(c). A variation of the

"plug" approach however, begins with the wet etch step depicted in Figure 3(d) wherein, instead of the dry approach, a wet etch is utilized to remove the remaining oxide dielectric layer 25. As known in the art, a conventional wet etch process is isotropic, and for removing the oxide layer 25, may comprise aqueous hydrofluoric acid or hydrofluoric acid in a nonaqueous solvent that may include an ammonium fluoride buffer and/or surfactants, or other soluble etchants. As a result of the wet etch process depicted in Figure 3(d), there is a resultant "pullback"o f the oxide 25 remaining underneath the formed vertical nitride spacers 35a, 35b. The wet etch oxide pullback, shown as 39a, 39b, formed beneath the nitride spacers 35a, 35b may be highly controlled, and the pulled-back region can be "plugged" effectively during the subsequent nitride deposition/etch processing. As shown in Figure 3(e), a thin nitride "plug" layer 40 is deposited over the remaining structure including the exposed gate and substrate surfaces. Preferably the thin nitride plug is 100Åor less, in thickness, and may include, though not limited to, Si_3N_4, Si_xN_y, carbon-containing Si_xN_y, an oxynitride, or a carbon-containing oxynitride.

[0038] After deposition, the nitride "plug"l yer 40 is etched using

a dry etch (e.g., RIE or CDE) which removes the layer on top of the gate and substrate surfaces, as shown in Figure 3(f). However, as a result of this process, thin nitride "plugs"45a, 45b remain that function to encapsulate and seal the underlying oxide dielectric portions 39a, 39b.

[0039] Once the dielectric portions are sealed, the lengthy strip may be performed during the subsequent silicide preclean (Figure 3(g)) without the creation of an oxide undercut.

[0040] In another embodiment of the invention, the thin nitride plug layer can be etched using wet chemistry (with hot phosphoric acid, hydrofluoric acid in ethylene glycol, or other well know nitride etches) such that the nitride is removed everywhere except in the regions that serves to seal and encapsulate the underlying dielectric (i.e. the "plug"r gion).

[0041] Finally, as depicted in Figure 3(h), the silicide contacts 60a, 60b are formed at each source/drain diffusion region utilizing a conventional silicidation process, as mentioned hereinabove. Optionally, a silicide contact 70 may be formed at top of gate stack 15. Then the contact etch stop (or barrier) film 80 is deposited as shown in Figure 3(h).

[0042] Advantageously, all three of the above-mentioned problems highlighted in the prior art process depicted in Fig-

ures 1(a)-1(d) for the conventional CMOS process are solved.

[0043] While the invention has been particularly shown and described with respect to illustrative and preformed embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention which should be limited only by the scope of the appended claims.